IN THE CLAIMS

Kindly amend independent claims 1 and 12 as shown in the attached claim listing:

1. (Currently Amended) A high power Doherty amplifier circuit having at least one input terminal and at least one output terminal comprising:

at least one carrier transistor forming a main amplifier stage;

at least one peak transistor forming a peak amplifier stage;

a first input line connecting the input terminal to an input of the carrier transistor and comprising an artificial transmission line;

a second input line connecting the input terminal to an input of the peak transistor and comprising an artificial transmission line;

a first output line connecting the output terminal to an output of the carrier transistor; and

a second output line connecting the output terminal to an output of the peak transistor, wherein the carrier transistor and the peak transistor are connected to a control circuit providing the desired dynamic controlling of amplification class parameters of the transistors.

2. (Original) The circuit of claim 1, wherein the first input line includes an inductor.

3. (Original) The circuit of claim 1, wherein the second input line comprises serial circuits and/or parallel circuits of at least one capacitance and / or at least one inductance.

4. (Original) The circuit of claim 3, wherein the second input line comprises an inductor.

5. (Original) The circuit of claim 1, wherein the first output line comprises serial circuits and/or parallel circuits of at least one capacitance and / or at least one inductance.

6. (Original) The circuit of claim 5, wherein the first output line comprises an inductor.

7. (Original) The circuit of claim 1, wherein the second output line comprises an inductor.

8. (Original) The circuit of claim 1, wherein the carrier transistor and the peak transistor have individual transconductance parameters and threshold voltage values.

9. (Original) The circuit of claim 1, wherein the carrier transistor output and the peak transistor output are each connected to a compensation circuit.

10. (Original) The circuit of claim 1, wherein an impedance transformation circuit is connected between the input terminal /output terminal and the input line/output line.

11. (Cancelled)

12. (Currently Amended) A high power Doherty amplifier circuit package comprising:

a support structure supporting circuit elements of the Doherty amplifier circuit;

at least one input terminal and at least one output terminal both terminals being supported on the support structure;

at least one carrier transistor forming a main amplifier stage and at least one peak transistor forming a peak amplifier stage both transistors being supported on the support structure;

a first input line connecting the input terminal to an input of the carrier transistor;

a second input line connecting the input terminal to an input of the peak transistor;

a first output line connecting the output terminal to an output of the carrier transistor and comprising an artificial transmission line; and

a second output line connecting the output terminal to an output of the peak transistor and comprising an artificial transmission line, wherein the carrier transistor and the peak transistor are connected to a control circuit providing the desired dynamic controlling of amplification class parameters of the transistors.

13. (Original) The package of claim 12, wherein the input and output lines are artificial transmission lines comprising serial circuits and / or parallel circuits of at least one capacitance and / or at least one inductance.

14. (Previously Presented) The package of claim 12, wherein a compensation circuit is connected to the output of at least one of the carrier transistor and the peak transistor.

15. (Previously Presented) The package of claim 14, wherein the compensation circuit comprises a serial circuit and/or a parallel circuit of at least one inductance and/or at least one capacitance.

16. (Original) The package of claim 12, wherein inductances are made up by bond wires provided between the transistors and the input and output terminals respectively.

17. (Original) The package of claim 12, wherein the input lines comprise parallel bond wires of a given length.

18. (Cancelled)